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MR

Docket No.: 60188-028 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Toshio YAMADA	:	
Serial No.: (Divisional of Serial No. 09/102,166)	:	Group Art Unit:
Filed: February 09, 2001	:	Examiner:

For: SEMICONDUCTOR INTEGRATED CIRCUIT, COMPUTER SYSTEM, DATA PROCESSOR AND DATA PROCESSING METHOD

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, DC 20231

Sir:

Prior to examination of the above-referenced application, please amend the application as follows:

IN THE CLAIMS:

Please amend claims 14 and 15 as follows:

14. (Amended) The computer system [,the data processor or the data processing method] of Claim [1, 2, 3 , 4 ,] 5[, 10, 12 or 13],

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wherein said memory network has a bus network structure.

15. (Amended) The computer system [,the data processor or the data processing method] of Claim [1, 2, 3 , 4 ,] 5[, 10, 12 or 13],

wherein said memory network has a ring network structure.